Supplying your technology needs

• Global Representative & Business Development Company
  – Semiconductor IP
  – SW Solutions and Applications
  – Chips / KDG
  – Modules

• Complex Technology Portfolio:
  – Wireless
  – Cellular
  – Consumer
  – Interface
  – General Purpose

• Industry Experts in the Wireless/Mobile & Consumer/DTV markets
  – IP, Semiconductors, OEM’s and Carriers
Our Markets

Wireless Mobile Communication Digital Consumer

Semiconductors Reference Designs Platform Partners

OEM ODM Design House

IP Semiconductor SW

Modules White Label PCBA

Network Operator

December 2012

T2M Product Portfolio
## Product Summary - IPs, SoC, Die

<table>
<thead>
<tr>
<th>Wireless IP</th>
<th>Interface IP</th>
<th>DTV Demod IP</th>
<th>Chips / Die</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bluetooth 2.1, 3.0, 4.0 – Mac/Phy/Modem</td>
<td>MIPI CNTRL / PHY</td>
<td>DVB-T2/T</td>
<td>2G/3G/4G RF Transceiver</td>
</tr>
<tr>
<td>Bluetooth Muli-mode, Single-mode – RF</td>
<td>USB 2.0/3.0 CNTRL / PHY</td>
<td>DVB-C2/C</td>
<td>802.11 B/G RF Transceiver</td>
</tr>
<tr>
<td>WiFi 802.11 A/B/G/N/AC - Mac/Phy/Modem</td>
<td>HDMI 1.3 / 1.4</td>
<td>DVB-S2/S</td>
<td>802.11 N/AC 2x3 5GHz RF</td>
</tr>
<tr>
<td>WiFi 802.11 A/B/G/N/AC – RF</td>
<td>SDIO, UHS-II, SlimBus, I2S-SC</td>
<td>DTMB</td>
<td>802.11 N 1x1 SoC</td>
</tr>
<tr>
<td>WiGig 802.11 AD – Mac/Phy/Modem</td>
<td>Encryption &amp; Security IP</td>
<td>ATSC</td>
<td>802.11 N 2X2 SoC</td>
</tr>
<tr>
<td>GPS / Glonass - BB</td>
<td>NFC PS SW</td>
<td>ISDB-T</td>
<td>WiMax SoC</td>
</tr>
<tr>
<td>GPS / Glonass - RF</td>
<td>NFC IP</td>
<td>ATSC M-H</td>
<td>WiMax System Modules</td>
</tr>
<tr>
<td>FM Receiver BB / RF</td>
<td>SSD-Controller</td>
<td>CMMB</td>
<td>ZigBee SoC</td>
</tr>
<tr>
<td>ZigBee BB / RF</td>
<td>RISC Processor Cores</td>
<td>DTV RF</td>
<td>GPS/Glonass SoC</td>
</tr>
<tr>
<td>LTE Phy / Modem / PS SW</td>
<td>DSP Cores</td>
<td>JPEG 2000-4K enc</td>
<td>Noise Suppression SoC</td>
</tr>
<tr>
<td>WiMax Phy / Modem / PS SW</td>
<td>8051, 80251 Cores</td>
<td>DVB Demodulator SoC</td>
<td></td>
</tr>
<tr>
<td>UMTS Phy / Modem / PS SW (TBD)</td>
<td>Memory Controllers</td>
<td>NFC Radio Controller SoC</td>
<td></td>
</tr>
<tr>
<td>GSM Phy / Modem / PS SW</td>
<td>DISPLAY CTRL 4K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise Cancellation / Suppression SW</td>
<td>SREDES</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Motion Processing / Sensor Fusion SW</td>
<td>PLLs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADC/DAC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Complex IPs, Chips, KGD**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Complex Wireless Connectivity IPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>802.11-G-Soc-IP</td>
<td>Complete 802.11G RF &amp; Digital IP for SoC integration</td>
</tr>
<tr>
<td>802.11-N-Soc-IP</td>
<td>Complete 802.11N RF &amp; Digital IP for SoC integration</td>
</tr>
<tr>
<td>802.11-AC-Soc-IP</td>
<td>Complete 802.11AC RF &amp; Digital IP for SoC integration</td>
</tr>
<tr>
<td>BT-2/3/4-MultiMode-Soc-IP</td>
<td>Complete Bluetooth Multi-Mode RF, Digital, &amp; SW for SoC Integration</td>
</tr>
<tr>
<td>BT-LE-Soc-IP</td>
<td>Complete Bluetooth Low Energy Single Mode RF, Digital &amp; SW for SoC Integration</td>
</tr>
<tr>
<td>802.11-N-RFIP</td>
<td>802.11-N 1x1 RF IP silicon proven in TSMC 65nm, supports 1x1 to 4x4</td>
</tr>
<tr>
<td>802.11-AC-RFIP</td>
<td>802.11-AC 2x3 RF IP silicon proven in TSMC 65nm, supports 1x1 to 4x4</td>
</tr>
<tr>
<td>BT-LE RF IP</td>
<td>BlueTooth Low Energy Only RF IP Silicon Proven in UMC 90nm</td>
</tr>
<tr>
<td>BT-Classic RF IP</td>
<td>BlueTooth Classic RF IP Silicon Proven in TSMC 90nm</td>
</tr>
<tr>
<td>BT-4.0 MultiMode-RF IP</td>
<td>BlueTooth 2/3/4/LE RF IP Silicon Proven in TSMC 90nm</td>
</tr>
<tr>
<td>GPS-RFIP</td>
<td>GPS RF IP Silicon Proven TSMC 90nm</td>
</tr>
<tr>
<td>GPS/Glonass-Soc-IP</td>
<td>Complete GPS/Glonass RF &amp; Digital IP for SoC integration</td>
</tr>
<tr>
<td>GPS/Glonass/Galileo/Comp ass/SAAS-DSP-FW-IP</td>
<td>Multi standard positioning DSP FW implementation</td>
</tr>
<tr>
<td>FM-Soc-IP</td>
<td>Complete FM Demodulator / Transmitter RF &amp; Digital IP for SoC integration</td>
</tr>
<tr>
<td>GSM/GPRS/EDGE-IP</td>
<td>GSM/GPRS/EDGE Digital &amp; SW PS IP</td>
</tr>
<tr>
<td>LTE-eNodeB-IP</td>
<td>LTE eNodeB Release 9 Digital &amp; PS SW IP</td>
</tr>
<tr>
<td>LTE-UE-IP</td>
<td>LTE UE Release 9 Digital &amp; PS SW IP</td>
</tr>
<tr>
<td>NFC-Radio-Controller-IP</td>
<td>NFC Radio Controller RF, Analog, Digital, FW IP for SoC integration</td>
</tr>
<tr>
<td>SSD-Controller-IP</td>
<td>Solid State Disk Drive flexible IP</td>
</tr>
<tr>
<td>WiMax-IP</td>
<td>802.11D &amp; E Wimax Digital IP for SoC integration</td>
</tr>
<tr>
<td>WiGig-IP</td>
<td>60GH WiGig Digital design IP for SoC Integration</td>
</tr>
<tr>
<td>ZigBee-802.15.4-Soc-IP</td>
<td>Complete IEEE802.15.4 ZigBee compliant RF, BaseBand, MAC &amp; SW IP for SoC integration</td>
</tr>
<tr>
<td>Display-Processor-IP</td>
<td>Quad Full HD / 3D Full HD Display Processor</td>
</tr>
<tr>
<td>Display-Ctrl-IP</td>
<td>High Resolution Display Controller</td>
</tr>
<tr>
<td>Display-Ctrl-4K-IP</td>
<td>Digital Cinema Display Controller (4K) for HDMI, DVI and DisplayPort transmitters</td>
</tr>
<tr>
<td>Display-Ctrl-Video-OUT-IP</td>
<td>Video Display Controller with Video Out IP</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Complex Digital TV Demodulator IPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>DTV-ATSC-IP</td>
<td>ATSC Demodulator Core - US DTV standard</td>
</tr>
<tr>
<td>DTV-ATSC-MH-IP</td>
<td>ATSC MH Mobile Demodulator Core - US MDTV standard</td>
</tr>
<tr>
<td>DTV-CMMB-Demod-IP</td>
<td>A complete CMMB Demodulator design</td>
</tr>
<tr>
<td>DTV-DTMB-IP</td>
<td>DTMB Demodulator Core - China DTV standard</td>
</tr>
<tr>
<td>DTV-DVBC-C-IP</td>
<td>DVBC-Demodulator Core - Cable DTV standard</td>
</tr>
<tr>
<td>DTV-DVBC-C2-IP</td>
<td>DVBC-C2 Demodulator Core - Cable DTV standard</td>
</tr>
<tr>
<td>DTV-DVBC-S-IP</td>
<td>DVBS demodulator / DSNG demodulator</td>
</tr>
<tr>
<td>DTV-DVBS2/S-IP</td>
<td>DVBS2/S Demodulator Core - Satellite DTV standard</td>
</tr>
<tr>
<td>DTV-DVBT/H-IP</td>
<td>DVBT/H Demodulator Core - Terrestrial DTV standard</td>
</tr>
<tr>
<td>DTV-ISDB-T/S-IP</td>
<td>ISDB-T/S Demodulators (full-seg or one-seg)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Processor Code Compatible Cores IPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>P320-IP</td>
<td>16-bit fixed point DSP - TMS320C25 series code compatible</td>
</tr>
<tr>
<td>P5602-IP</td>
<td>8Bit Processor soft core - 6502 code compatible</td>
</tr>
<tr>
<td>P68000-IP</td>
<td>32Bit Processor soft core - Motorola 68000 code compatible</td>
</tr>
<tr>
<td>P80186-IP</td>
<td>16-bit Microcontroller - 80186 series code compatible</td>
</tr>
<tr>
<td>P80251-IP</td>
<td>8Bit Processor soft core - 80251 code compatible</td>
</tr>
<tr>
<td>P8051-IP</td>
<td>8Bit Processor soft core - 8051 code compatible</td>
</tr>
<tr>
<td>P7TDMi-IP</td>
<td>32Bit Risc Processor soft core - ARM 7 code compatible</td>
</tr>
<tr>
<td>P9TDMi-IP</td>
<td>32Bit Risc Processor soft core - ARM 9 code compatible</td>
</tr>
<tr>
<td>P280-IP</td>
<td>8Bit Processor soft core - 280 code compatible</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Chips or KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>NFC Chip</td>
<td>NFC Radio Controller Chip, EMVco Certified</td>
</tr>
<tr>
<td>ZigBee-802.15.4-Soc-Chips</td>
<td>Fully functional single chip ZigBee SoC</td>
</tr>
<tr>
<td>BT Chip</td>
<td>BT Classic Single Chip SoC</td>
</tr>
<tr>
<td>802.11AC 5GHz RF</td>
<td>802.11N/AC 5GHz Only 2x3 RF chip or die in 65nm TSMC</td>
</tr>
<tr>
<td>802.11N SoC chips</td>
<td>802.11N - 1x1, 2x2 SoC with integrated RF</td>
</tr>
<tr>
<td>802.11AC SoC chips</td>
<td>802.11AC - 1x1, 2x2 SoC with integrated RF</td>
</tr>
<tr>
<td>WiMax D &amp; E Chips</td>
<td>802.11D &amp; E Wimax Digital IP for SoC integration</td>
</tr>
<tr>
<td>GPS / Glonass Chips</td>
<td>GPS, GPS+Glonass Digital BaseBand, RF &amp; Module</td>
</tr>
<tr>
<td>2G/3G/4G RF Transceiver</td>
<td>Single Chip, DigRF interface, LTE, UMTS, TD-SCDMA, GGE</td>
</tr>
<tr>
<td>Noise Suppression Chip</td>
<td>Noise Suppression &amp; Echo Cancelation for cell phones, tablets etc.</td>
</tr>
<tr>
<td>DVB-T Chip</td>
<td>DVB-T SoC with integrated RF, Demodulator, USB and TS</td>
</tr>
</tbody>
</table>
# Interface IPs

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Interface IPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2-Transceiver-IP</td>
<td>High Performance DDR2 Transceiver</td>
</tr>
<tr>
<td>DDR2/3-Controller-IP</td>
<td>DDR2/3 Memory Controller</td>
</tr>
<tr>
<td>ETHERNET-MAC-1G-IP</td>
<td>Gigabit Ethernet Media Access Controller IP</td>
</tr>
<tr>
<td>ETHERNET-MAC-1G-Lite-IP</td>
<td>Gigabit Ethernet Media Access Controller - Lite IP</td>
</tr>
<tr>
<td>ETHERNET-MAC-1G-PCI-IP</td>
<td>Gigabit Ethernet Access Controller with PCI Interface IP</td>
</tr>
<tr>
<td>ETHERNET-MAC-1G-PCS-IP</td>
<td>Gigabit Ethernet Access Controller Physical Coding Sublayer IP</td>
</tr>
<tr>
<td>ETHERNET-MAC-FAST-IP</td>
<td>Fast Ethernet MAC IP</td>
</tr>
<tr>
<td>HDMI-1.3-RX-IP</td>
<td>HDMI 1.3 Receiver IP</td>
</tr>
<tr>
<td>HDMI-1.3-RX-PHY-IP</td>
<td>HDMI 1.3 Receiver PHY IP for HDMI Rx applications</td>
</tr>
<tr>
<td>HDMI-1.3-TX-IP</td>
<td>HDMI 1.3 Transmitter IP</td>
</tr>
<tr>
<td>HDMI-1.3-TX-PHY-IP</td>
<td>HDMI 1.3 Transmitter PHY IP for HDMI Tx applications</td>
</tr>
<tr>
<td>HDMI-1.4-RX-IP</td>
<td>HDMI 1.4 Receiver IP</td>
</tr>
<tr>
<td>HDMI-1.4-RX-PHY-IP</td>
<td>HDMI 1.4 Receiver PHY IP for HDMI Tx applications</td>
</tr>
<tr>
<td>HDMI-1.4-TX-IP</td>
<td>HDMI 1.4 Transmitter IP</td>
</tr>
<tr>
<td>HDMI-1.4-TX-PHY-IP</td>
<td>HDMI 1.4 Transmitter PHY IP for HDMI Tx applications</td>
</tr>
<tr>
<td>I2C-IP</td>
<td>I2C Compatible Bus Controller</td>
</tr>
<tr>
<td>I2S-IP</td>
<td>I2S Compatible Bus Controller</td>
</tr>
<tr>
<td>MIPI-Controller-Rx-CS12-IP</td>
<td>MIPI Controller - CSI Receiver</td>
</tr>
<tr>
<td>MIPI-Controller-Tx-CS12-IP</td>
<td>MIPI Controller - CSI2 Transmitter</td>
</tr>
<tr>
<td>MIPI-Controller-UFS-Device-IP</td>
<td>MIPI Controller - UFS UTP Device</td>
</tr>
<tr>
<td>MIPI-Controller-UFS-Host-IP</td>
<td>MIPI Controller - UFS HOST</td>
</tr>
<tr>
<td>MIPI-Controller-UNIPRO-IP</td>
<td>MIPI Controller - UNIPRO</td>
</tr>
<tr>
<td>MIPI-D-Phy-Controller</td>
<td>MIPI D-Phy &amp; MDDI configurable IP for Display interface applications</td>
</tr>
<tr>
<td>MIPI-D-Phy-Rx-CS1-IP</td>
<td>MIPI D-Phy Receiver for Camera Interface applications (CSI)</td>
</tr>
<tr>
<td>MIPI-D-Phy-Rx-DSI-IP</td>
<td>MIPI D-Phy Receiver for Display Interface applications (DSI)</td>
</tr>
<tr>
<td>MIPI-D-Phy-Rx-LVDS-DSI-IP</td>
<td>MIPI D-Phy Receiver compatible with the TIA/EIA-644 LVDS standard for Display Interface applications (DSI)</td>
</tr>
<tr>
<td>MIPI-D-Phy-Transceiver-IP</td>
<td>MIPI D-Phy Transmitter &amp; Receiver IP for connecting Camera &amp; Display devices to a host processor</td>
</tr>
<tr>
<td>MIPI-D-Phy-Tx-CS12-IP</td>
<td>MIPI D-Phy Transmitter for Camera interface applications (CSI2)</td>
</tr>
<tr>
<td>MIPI-D-Phy-Tx-DSI-IP</td>
<td>MIPI D-Phy Transmitter for Display interface applications (DSI)</td>
</tr>
<tr>
<td>MIPI-DigRF-v4.0-IP</td>
<td>MIPI Phy for 4G/3G/2G RF Interfaces</td>
</tr>
<tr>
<td>MIPI-LVDS-Receiver-IP</td>
<td>LVDS MIPI Receiver</td>
</tr>
<tr>
<td>MIPI-M-Phy-IP</td>
<td>MIPI M-Phy for interfacing to display, camera, audio, video, memory, power management and Baseband to RFIC</td>
</tr>
<tr>
<td>MIPI-PHY-IP</td>
<td>High performance PLL based frequency synthesizer for MIPI applications</td>
</tr>
<tr>
<td>MIPI-SLIMBus-Dev-Controller-IP</td>
<td>MIPI SLIMBus Device Controller</td>
</tr>
</tbody>
</table>

## Interface IPs cont.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Interface IPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI-2.2-Transceiver-IP</td>
<td>PCI 2.2 compliant Transceiver Phy</td>
</tr>
<tr>
<td>PCI-X-Transceiver-IP</td>
<td>High Performance PCI-X Transceiver</td>
</tr>
<tr>
<td>SD-2.0-HOST-Controller-AHB-IP</td>
<td>SD 2.0 Host Controller IP with AHB/OCP/VCI Amster/Slave Interface</td>
</tr>
<tr>
<td>SD-3.0-HOST-Controller-IP</td>
<td>SD 3.0 Host Controller IP with AHB/OCP/VCI Interface</td>
</tr>
<tr>
<td>SD/SDIO/MMC/eMMC-HOST-Controller-IP</td>
<td>SD/SDIO/eMMC/MMC Host Controller IP</td>
</tr>
<tr>
<td>SDIO-2.0-DEVICE-Controller-AHB-IP</td>
<td>SDIO 2.0 Device Controller IP with AHB interface</td>
</tr>
<tr>
<td>SDIO-3.0-DEVICE-Controller-AHB-IP</td>
<td>SDIO 3.0 Device Controller IP with AHB interface</td>
</tr>
<tr>
<td>SDLC-IP</td>
<td>Synchronous Data Link Control Protocol Controller IP</td>
</tr>
<tr>
<td>SDXC-eMMC-Multislot-IP</td>
<td>SDXC multi card reader with proven SDR104 support</td>
</tr>
<tr>
<td>UCB-Transceiver-IP</td>
<td>High Performance Universal CardBus Transceiver</td>
</tr>
<tr>
<td>SmartCard-Controller-IP</td>
<td>Smart Card Interface Controller</td>
</tr>
<tr>
<td>SPDIF-IP</td>
<td>Sony/Philips Digital Interface Controller</td>
</tr>
<tr>
<td>SPI-IP</td>
<td>Serial Peripheral Interface IP</td>
</tr>
<tr>
<td>UART-IP</td>
<td>UART</td>
</tr>
<tr>
<td>UHS-II-PHY-IP</td>
<td>PHY IP solution for UHS-II interface</td>
</tr>
<tr>
<td>US2.0-DS-Dev-Ctrl+Proc-IP</td>
<td>USB 2.0 Full Speed Device Controller with embedded 8051 controller IP</td>
</tr>
<tr>
<td>US2.0-DS-Dev-Ctrl-IP</td>
<td>USB 2.0 Full Speed Device Controller</td>
</tr>
<tr>
<td>US2.0-HS-Device-IP</td>
<td>USB 2.0 Hi-Speed Device Controller</td>
</tr>
<tr>
<td>US2.0-HS-HOST-IP</td>
<td>USB 2.0 Hi-Speed HOST Controller with EHCI and OHCI interface</td>
</tr>
<tr>
<td>US2.0-HS-Hub-IP</td>
<td>USB 2.0 Hi-Speed Hub Controller</td>
</tr>
<tr>
<td>US2.0-HS-IC-Phy-IP</td>
<td>USB 2.0 High Speed Inter Chip PHY</td>
</tr>
<tr>
<td>US2.0-OTG-Multi-Device-IP</td>
<td>USB 2.0 High Speed OTG Multiple Peripheral Device Controller</td>
</tr>
<tr>
<td>US2.0-OTG-HS-Device-IP</td>
<td>USB 2.0 High Speed On-The-Go Single Device Controller</td>
</tr>
<tr>
<td>US2.0-Phy-IP</td>
<td>USB 2.0 High, Full and Low Speed PHY</td>
</tr>
<tr>
<td>US3.0-Device-Controller-IP</td>
<td>USB 3.0 Device Controller</td>
</tr>
<tr>
<td>US3.0-Device-Controller-RNDIS-IP</td>
<td>USB 3.0 device contyroller with an integrated RNDIS bridge</td>
</tr>
<tr>
<td>US3.0-Dual-Mode-Controller-IP</td>
<td>USB 3.0 Dual Mode Controller</td>
</tr>
<tr>
<td>US3.0-Host-Controller-IP</td>
<td>USB 3.0 Host Controller</td>
</tr>
<tr>
<td>US3.0-Hub-Controller-IP</td>
<td>USB 3.0 Hub Controller</td>
</tr>
<tr>
<td>US3.0-Phy-IP</td>
<td>USB 3.0 Phy IP for SoC Integration</td>
</tr>
<tr>
<td>US3.0-SS-Dev-Ctrl-IP</td>
<td>USB 3.0 SuperSpeed Device Controller</td>
</tr>
</tbody>
</table>
## Security and General IPs

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Security and Encryption IPs</th>
<th>Part Number</th>
<th>General Purpose IPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>3DES-EN-IP</td>
<td>Data Encryption Standard (DES/3DES) Core</td>
<td>AC97-Controller-IP</td>
<td>AC97 Controller</td>
</tr>
<tr>
<td>AES-CCM-WBOA-IP</td>
<td>WPAN MBOA MAC AES CCM Core</td>
<td>ADC-LP-10b-IP</td>
<td>10-bit Low Power ADC</td>
</tr>
<tr>
<td>AES-CCM-WMax-IP</td>
<td>IEEE 802.16e (WiMAX) AES Core</td>
<td>ADC-LP-9b-IP</td>
<td>9-bit Low Power ADC</td>
</tr>
<tr>
<td>AES-CCM-WLAN-IP</td>
<td>802.11i CCM (CTR+CBC) AES Core for WiFi WLAN</td>
<td>ATA-IP</td>
<td>ATA, IDE, &amp; ATAPI Interface IP</td>
</tr>
<tr>
<td>AES-CCM-ZigBee-IP</td>
<td>IEEE 802.15.4 (ZigBee) CCM AES Cores</td>
<td>ATA-Transceiver-Parallel-IP</td>
<td>High Performance Parallel ATA Transceiver</td>
</tr>
<tr>
<td>AES-FIPS-IP</td>
<td>Advanced Encryption Standard (AES, FIPS-197) Core</td>
<td>BandGap-1V-Ref-IP</td>
<td>BandGap reference for 1V Power Supply</td>
</tr>
<tr>
<td>AES-GCM-IP</td>
<td>AES-GCM MACsec (IEEE 802.1AE) and FC-SP Cores</td>
<td>BandGap-Ref-IP</td>
<td>Bandgap Reference</td>
</tr>
<tr>
<td>AES-IP</td>
<td>NIST AES Key Wrap/Unwrap Core</td>
<td>BanGap-LVDET-2-IP</td>
<td>Dual Low-Voltage Detector</td>
</tr>
<tr>
<td>AES-XTS-IP</td>
<td>XTS-AES IEEE P1619 Core Families</td>
<td>DLL-IP</td>
<td>CMOS High Speed DLL IP</td>
</tr>
<tr>
<td>AES-XTS/GCM-IP</td>
<td>GCM/XEX/XTS AES Core P1619/802.1ae (MACSec)</td>
<td>HSTLIII-Transceiver-IP</td>
<td>High Performance HSTL III Transceiver</td>
</tr>
<tr>
<td>AES-XTS-LXP-IP</td>
<td>Lossless Compression Core with AES-XTS encryption /decryption - High Performance</td>
<td>HDCP-Transceiver-AHB-IP</td>
<td>HDCP 2.0 Transmitter / Receiver with AHB Slave interface</td>
</tr>
<tr>
<td>AES-XTS-LZR-IP</td>
<td>LZ Lossless Compression Core with AES-XTS encryption /decryption - High Performance</td>
<td>HDLC-IP</td>
<td>High-level Data Link Control Protocol Controller IP</td>
</tr>
<tr>
<td>ECC-IP</td>
<td>ECC - Elliptic Curve Point Multiply and Verify Core</td>
<td>LVDS-DS-4CH-IP</td>
<td>1.25 Gbps 4-Channel LVDS Deserializer</td>
</tr>
<tr>
<td>FEC-CC-IP</td>
<td>Forward Error Correction Codec for Cyclic Code (2112,2080) for 10G/40G/100G Ethernet MAC</td>
<td>LVDS-SR-4CH-IP</td>
<td>1.25 Gbps 4-Channel LVDS Serializer with Pre-emphasis</td>
</tr>
<tr>
<td>FEC-LDPC-IP</td>
<td>LCPC Forward Error Correction for G.9960</td>
<td>LVDS-Transceiver-IP</td>
<td>666 Mbps LVDS Transceiver IP</td>
</tr>
<tr>
<td>FEC-RS-IP</td>
<td>Reed-Solomon Forward Error Correction for IEEE 802.3bj (100 Gbps Ethernet)</td>
<td>LVDS-Transceiver-MDDI-IP</td>
<td>LVDS VESA MDDI Transceiver</td>
</tr>
<tr>
<td>FFT-DSP-IP</td>
<td>FFT DSP Core for up to 4096 Points</td>
<td>MDDI-T2-PHY-IP</td>
<td>MDDI Type 2 Compliant PHY IP</td>
</tr>
<tr>
<td>IPSec-IP</td>
<td>IPSec Security Processor</td>
<td>MDDR-I/F-IP</td>
<td>Mobile DDR SDRAM Memory I/F IP mDDRC 333A</td>
</tr>
<tr>
<td>KSM-ENC-IP</td>
<td>Kasumi Encryption Core</td>
<td>MUX-4l/p-IP</td>
<td>High Frequency, High Performance 4-input Analog MUX</td>
</tr>
<tr>
<td>PRNG-IP</td>
<td>Cryptographically Secure Pseudo Random number Generator IP Core</td>
<td>NAND-Flash-Ctrl-IP</td>
<td>NAND Flash Memory Controller</td>
</tr>
<tr>
<td>RC4-IP</td>
<td>RC4 Keystream Generator</td>
<td>PLL-CDR-IP</td>
<td>Clock/Data Recovery PLL</td>
</tr>
<tr>
<td>RSA-IP</td>
<td>RSA Public Key Exponentiation Accelerator Core</td>
<td>PLL-FRAC-N-IP</td>
<td>Fractional N-PLL</td>
</tr>
<tr>
<td>SNOW3G-ENC-IP</td>
<td>SNOW 3G Encryption Core</td>
<td>PLL-SS-IP</td>
<td>Spread Spectrum PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PLL-SYNTH-IP</td>
<td>Frequency Synthesizer PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PLL-SYNTH-LF-IP</td>
<td>32KHz input frequency Synthesizer PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SERDES-2500A-IP</td>
<td>2.5 Gbps Transceiver core</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SERDES-3204-IP</td>
<td>3.25 Gigabit SerDes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SERDES-EPOP-IP</td>
<td>1.25 Gbps EPON SerDes IP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SERDES-SGMII-1.25Gbps-IP</td>
<td>1.25 Gbps Serial Gigabit Media Independent Interface SerDes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SSL-Transceiver-Phy-IP</td>
<td>High Frequency, High Performance SSL Transceiver Phy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SRAM-Compiler</td>
<td>SRAM Compiler</td>
</tr>
</tbody>
</table>

**December 2012**

**T2M Product Portfolio**
# Table Of Contents

- Wireless Connectivity  
  Page 11
- 802.11 A/B/G/N/AC: Solutions  
  Page 12
- Bluetooth MAC/MODEM/RF 2.1/3.0/4.0 Solutions  
  Page 13
- GPS IP Solutions  
  Page 14
- LTE MAC-Phy, Protocol Stack SW  
  Page 15
- WiMax – IP, Chips, Die, Modules  
  Page 16
- 3G PS SW – Terminal and Femtocell  
  Page 17
- GSM MAC/PHY/MODEM & PS SW  
  Page 18
- Multimode 2G/3G/4G RF Transceiver IC Solutions  
  Page 19
- Motion Solutions for Mobile Phones  
  Page 20
- Noise Suppression for Mobile Phones – Chips & IP  
  Page 21
- Digital TV Demod IP, Chips, Die  
  Page 24
- MIPI Interface controllers and PHY IP availability  
  Page 26
- MIPI interface IP solutions  
  Page 27
- USB, Memory, Multimedia and 8051  
  Page 28
- SDIO, USB, SLIMBUS  
  Page 29
- HDMI IP & Chip Portfolio  
  Page 30
- UHS-II IP Portfolio  
  Page 31
- NFC Radio Controller IP, Chip, Die  
  Page 32
- NFC Protocol Stack SW  
  Page 33
- Security & Encryption IP Cores  
  Page 34
- Storage IP : Programmable SSD Flash Controller IP  
  Page 35
- RISC Processor Cores  
  Page 36
- DSP Processor Cores  
  Page 37
1. T2M
2. Wireless Products
3. Consumer Products
4. Interface Products
5. Contact Us
## Wireless Connectivity

### WiFi-MAC/PHY
- 802.11 A/B/G
- 802.11 N 4x4
- 802.11 AC 4x4
- 802.11 AD (WiGig – 60GHz)

### Bluetooth - Mac/PHY/Modem/PS SW/Profiles
- BT 2.1+EDR
- BT 4.0 MultiMode
- BT 4.0 Low Energy single mode
- BT LE PS SW

### ZigBee
- 802.15.4 BB/Modem/RF – 180nm CMOS

### GPS / Glonass - BB
- GPS / GLONASS - BB

### FM Transceiver
- FM Transceiver BB + RF - 90/95/40nm TSMC

### Connectivity - RF
- WiFi 802.11 N/AC 2x3 RF - 65nm TSMC
- BT 2.1, EDR, 4.0 LE RF - 90nm TSMC
- BT 4.0 Multimode RF - 90nm TSMC
- BT LE only - 90nm UMC
- GPS / Glonass RF - 90nm TSMC
802.11 A/B/G/N/AC: Solutions

- **802.11abg MAC /modem - Certified and in mass production**
  - 11abgh all digital MAC + Modem logic with Analog I/F to external RF
  - Compatible with external WiFi Radios like Maxim 2829/30 or Airoha AL2236

- **802.11 N/AC MAC /modem**
  - Architecture designed for scalability, upgradability and performance
  - MAC is scalable to support from 11n 1x1 up to 11ac 4x4!
    - 802.11n 1x1 20 & 40 MHz , 802.11n 3x3 40 MHz
    - 802.11ac 1x1 40 MHz , 802.11ac 80 MHz
  - All Digital IP for SoC integration
  - Analog Interface to WiFi transceiver in TSMC 40nm and other technologies

- **802.11 N/AC RF Transceiver IP in TSMC 65nm**
  - Available as Silicon IP, Die or packaged part (2x3)
  - IP can be configured as 1x1 up to 4x4 in any combination
  - Integrated PA and fully integrated synthesizer, Support for external PA (driver on-chip)
  - On-chip balun & matching on RX/TX
  - On-chip antenna switch for TX and RX0
  - 8.6MM2 die in TSMC CMOS 65 nm LP (1P6M, 1.2V/2.5V)

- **802.11 N chips or Die**
  - 802.11N/AC 2x3, 5GHz, 20/40Mhz bandwidth, I/Q Interface, RF Transceiver with integrated PA
  - 802.11N 2x2, 300Mbps, 20/40Mhz bandwidth, PCI Express Interface, PA+RF+Digital SoC
  - 802.11N 1x1, 150Mbps, 20/40Mhz bandwidth, USB 2.0 Interface, PA+RF+Digital SoC
Bluetooth MAC/MODEM/RF 2.1/3.0/4.0 Solutions

**BT MAC/MODEM - 4.0 Dual Mode**
- Embeddable Bluetooth baseband core
  - Compliant with BT 1.2, BT 2.0+EDR, BT 2.1+EDR, BT 3.0 and BT 4.0 LE
  - Hardware core: RTL source code
  - Software protocol stack up to HCI: C source code
  - Including digital modem (GFSK; π/4-DQPSK; 8-DPSK)
- Provided with logic for voice applications:
  - CVSD hardware codec, A-law / u-law / linear converter, PCM interface
- Provided with WLAN and broadband co-existence interface

**BT MAC/MODEM/SW/PROFILES - 4.0 Single Mode**
- Embeddable Bluetooth baseband core
  - Compliant with BT 4.0 LowEnergy only
  - Including digital modem (GFSK; π/4-DQPSK; 8-DPSK)
  - Verilog RTL, provided with System Verilog test bench with regression
  - Including digital modem (GFSK; π/4-DQPSK; 8-DPSK)
- Full protocol stack - C Source Code
  - below HCI, dependence with hardware baseband
  - above HCI, with profiles, can also be used in combination with 3rd party HCI stand alone BLE IC

**BT RF - 4.0 Dual Mode (2/3/4)**
- Embeddable Bluetooth RF IP in TSMC 90nm LP RFCMOS
  - Compliant with BT 2.1+EDR, BT 3.0 and BT 4.0

**BT RF - 4.0 Single Mode (4.0 only)**
- Embeddable Bluetooth RF IP in UMC 90nm CMOS
  - Compliant with BT 4.0 Low Energy
GPS / GLONASS IP Solutions

GPS BASE-BAND FEATURES

• Correlator engine for both standalone GPS, GLONASS and AGPS
• 16 parallel tracking channels and massive acquisition correlators
• Sensitivity
  – Tracking –160dBm
  – Hot start –155dBm
  – Cold start –144dBm
• Industry best Time To First Fix
• Low Interrupt rate to the processor
• Power down scheme for individual channels to reduce the average power
• Built in Battery Backed Counter to maintain GPS time
• Popular AMBA Slave / SPI provides easy interface to host processor
• Fully synchronous design according to RMM guidelines
• Available as RTL

GPS SW FEATURES

• Standalone GPS receiver software with NMEA output
• Executable binary code for ARM7 available for GPS
• < 35MIPS on ARM7
LTE MAC-Phy, Protocol Stack SW

3GPP LTE UE Physical Layer and MAC-PHY Interface
- 3GPP LTE (release 9) PHY Baseband
- All Downlink and Uplink Physical Channels, Libraries, Algorithms
- Integrated with cross-functional logic as a single PHY solution and interfaced with MAC-PHY API.

3GPP LTE eNodeB Physical Layer and MAC-PHY Interface
- 3GPP LTE (release 9) eNodeB PHY Baseband and MAC-PHY API.
- PHY baseband covers all Downlink Transmitter and Uplink Receiver Physical Channels, Libraries, Algorithms
- Integrated with cross-functional logic as a single PHY solution and interfaced with MAC-PHY

General
- Algorithms are optimized and tested with standard 3rd party tier-1 IQ test vectors, test scenarios and interoperated in real-time with UE through RF interface.
- DL algorithms have been tested with 3GPP LTE Channel and propagation models for uplink receiver algorithms as per EPA, EVA and ETU for Doppler frequency 5-300Hz as defined by TS36.101 Annexure-B.

3GPP LTE UE Protocol Stack SW Solution
- Compliance with 3GPP LTE Release 9.
- TDD and FDD modes.
- UE category 1, 2, 3, 4, 5
- Portable to embedded HW-SW platforms
- All transmission bandwidths, transmission modes (SISO and MIMO) of LTE.

3GPP LTE eNodeB Protocol Stack SW Solution
- Fully scalable implementation supporting all types of small cell solutions (femto, enterprise femto, Pico)
  - Layer 2: MAC incl. UL & DL Scheduler, RLC, PDCP
  - Layer 3: RRC, B-RRM
  - IF: S1, X2, Local OAM
- Configurable multi-thread architecture for tailored integration on various platforms,
- Multicore / Multi CPU platform support
- SMP and AMP OS support

LTE Protocol Stack SW support and integration services
- Team of highly experienced SW design engineers with 100 man years of experience
- Design, Integration, test and validation services
WiMax – IP, Chips, Die, Modules

**WiMax IP**

- **RX baseband signal processing**
  - Receiver synchronization
  - Received signal processing (de-modulation)
  - Forward error control code decoding (outer receiver)
- **RX real-time packet processing**
  - Error packet detection (CRC)
  - IE content (MAP) parsing/decoding
  - CID filtering and PDU forwarding
- **TX real-time packet processing**
  - Error control insertion (CRC)
  - Data burst padding
  - Control message and MAP parsing
- **TX baseband signal processing**
  - Forward error control encoding
  - Constellation encoding, multi-carrier modulation
  - Spectrum shaping

**WiMax Chips & Die**

- **SS & Pico BS support, IEEE 802.16-2004**
- Adaptive Modulation, BPSK, QPSK, 16QAM, 64QAM
- Frame duration, 2.5, 5, 10, 20ms
- Channel Bandwidth, 1.25, 1.75, 2.5, 3, 3.5, 5, 6, 7, 10MHz
- Cyclic Prefix, Auto detect 1/4, 1/8, 1/16, 1/32
- UL subchannelization support
- QoS Class, UGS, rtPS, nrtPS, BE
- PKMv1 authentication and key exchange
- X.509 certificate & RSA/3DES mechanism
- AES-CCM & DES-CBC security engines
- **Interface**
  - Analog Differential I/Q RF interface
  - PCI/mini-PCI, MII/RMII, UART, SPI
- **Processor, ARM 926EJS @ 260MHz**

**WiMax Modules**

- single board for CPE: 5.8GHz, 3.5GHz, 450MHz
- mPCI for CPE: 2.3GHz, 3.5GHz, 5.8GHz, 450MHz
- USB modem: 2.3GHz, 3.5GHz
3G PS SW – Terminal and Femtocell

3G Terminal Protocol Stack SW
- Fully compliant Protocol Stack SW solutions for forming the foundation of a universal 3G handset
- Test and integration services
- Full ANSI-C Compliant

3G Femtocell PS SW
- Provides the complete solution for a standalone FAP, based upon a modern SoC femtocell chipset with PHY and Linux baseport provided by the chip manufacturers.
- All the key Radio Resource Management software managed:
  - Access Control
  - Congestion control and Dynamic RAB Management
  - Channel-type Switching
  - Quality of service
  - Code allocation management
  - Power control
  - Interference mitigation
  - Radio parameter auto-configuration

WCDMA:
- WCDMA(R99) : UL384K/DL384K
- WCDMA(R4/R5) : UL384K/DL3.6M
- CMCC(V1/V2/V3)

TD-SCDMA:
- TD-SCDMA(R4): UL128K/DL384K
- TD-HSPA(R5/R6/R7) : UL2.2M/DL2.8M

December 2012
T2M Product Portfolio
GSM MAC/PHY/MODEM & PS SW

MAC/PHY/MODEM

- General
  - Quad-Band GSM/GPRS/EDGE 850/900/1800/1900MHz
  - GSM release 4
  - GPRS/EDGE multi-slot class 12
  - Mobile station class B

- Data Properties
  - GPRS: max: 85.6Kbps
  - EDGE: Uplink or downlink max throughput: 236.8Kbps
  - Coding scheme: CS1~4, MCS1~9

- Voice Properties
  - Modem and stack support for Full Rate (FR) and Enhanced Full Rate (EFR)

- Stack Interface
  - Comprehensive AT Command I/F including Multiplexing to 3GPP 27.010
  - 3GPP 27.007 AT command set for User Equipment
  - 3GPP 27.005 Use of Data Terminal Equipment (SMS)

- RF Interface
  - Programmable RF interface supporting DigRF Ver 1.12 or digital 12bits/12bits I/Q interface.

- Clock Requirements
  - Low clock frequency 160MHz - 200MHz

- Deliverables
  - Verilog RTL code with synthesis scripts Test bench verification environment
  - Modem, L1 and PS software

- Maturity
  - Network proven
  - Silicon verified

Protocol Stack SW

- GSM/GPRS/EGPRS
  - Quad Band: 900, 1800, 850, and 1900
  - FR, HR, EFR, AMR speech
  - Class 1~12, Class B
  - Coding scheme CS 1 to 4; MCS 1 to 9
  - CSD (Trans, Non-trans) & Fax option
  - L1 Control and Driver sublayer

- Supplementary Services
  - AT-cmd interface (standard & enhanced)

- SMS supports Text and PDU mode

- Application development layer

- Ported onto 7 basebands to date
  - 500+ handset models; >1B production

- PTCRB/GCF validated
  - latest March ‘08 and TBA July ’09

- ANSI C code throughout
  - hand-coded for efficiency, low latency, and low footprint
  - modular, highly-structured design
  - fully instrumented; debug detail set by jHAT in real-time

- SIM Interface supports Phase 1 & 2 cards

- Portable Layer-1 design

- SIM Toolkit Option

- Nucleus PLUS RTOS and Nucleus Net TCP/IP stack
Multimode 2G/3G/4G RF Transceiver IC Solutions

**Multi-Mode 2G/3G/4G (Single Chip)**
- 2G/3G/4G RF Transceiver with DigRF 4G interface
- Supports LTE TDD/FDD, TD-SCDMA/HSPA all E-ULTRA Bands
- SAW less architecture
  - No interstage SAW in LTE FDD Mode or WCDMA Mode
  - No SAW in TD-SCDMA
- Sampling 4Q12

**Multi-Mode 2G/3G/4G (2 Chip)**
- 2G/3G/4G RF Transceiver with I/Q interface + ABB IC
- Supports LTE TDD/FDD, TD-SCDMA/HSPA, all E-ULTRA Bands
- Supports Dual Downlink, Single Uplink, Parallel Digital Interface
- SAW less architecture
  - No interstage SAW in LTE FDD Mode or WCDMA Mode
  - No SAW in TD-SCDMA

**Dual Mode 2G/3G with Support for Band 40**
- Supports GSM/UMTS/HSPA/TD-SCDMA/Band 40
- DigiRF3 interface, I/Q Interface, Parallel interface TD-SCDMA
- SAW less architecture

**Single Mode 3G Already in Production and On the Market**
- WCDMA, Millions Sold in Brand-Name Phones
- TD-SCDMA, Millions Sold in Brand-Name Phones
- SAW less architecture
Motion Solutions for Mobile Applications

“Selling good sensors is not good enough. It’s all about sensor fusion software!”

Jeremie Bouchard, Principal Analyst, IHS iSupply, May 2012

- **MotionEngine™ Mobile**: Sensor independent software solution that provides high performance calibration and sensor fusion for 6-axis and 9-axis devices.

- **Gesture Recognition Engine**: Software library of event gestures, character gestures and virtual controls plus an SDK that enables the developer to create custom gestures.

- **Context Awareness Library**: Uses motion data to interpret environment and determine context, allowing the device and applications to intelligently predict the needs of the user.

- **Cursor Library**: Software library that enables smartphones equipped with a gyroscope to precisely control a cursor on a Smart TV, PC or other device.
MotionEngine™ Mobile Implementations

MotionEngine™ on an App Processor

- Available on all major Apps Processors
- ARM / MIPS / Atom
- Android / WinMobile / Linux

MotionEngine™ in a Sensor Hub

- Available on all major sensor hub chips
- ARM / MIPS / 8051
- 32Bit / 16Bit / 8Bit
- Win8 certified
Noise Suppression for Mobile Phones (Chips & IP)

Talking in **NOISE** is **understood**
Voice Extraction & Noise Suppression

- Extracts speech from high background noise
- Suppresses background noise for listener
- Talker speech sent with improved intelligibility

Listening in **NOISE** is **easier**
Bright Voice Enhancement

- Enhances received voice above local noise
- Enhanced speech output to listener
- Talker hears and understands better
1. T2M
2. Wireless Products
3. Consumer Products
4. Interface Products
5. Contact Us
# Digital TV Demod IP, Chips, Die

## DTV Demodulator IP
- DVB-T2 / T
- DVB-S2 / S
- DVB-C2 / C
- DVB-C / J83
- ATSC
- DTMB
- Universal QAM/PSK demodulator

## DTV RF Tuner IP
- DVB-T2 / T
- DVB-S2 / S
- DVB-C2 / C
- DVB-C / J83
- ATSC
- DTMB

## MDTV Demodulator IP
- ATSC-M/H
- DVB-H
- CMMB

## MDTV RF Tuner IP
- ATSC-M/H
- DVB-H
- CMMB

## DTV Modulator IP
- DVB-T
- DVB-T2
- ISDB-T
- ATSC 8-VSB
- Universal QAM/PSK modulator

## Other
- Viterbi encoder/decoder
- Reed Solomon

## DTV Demodulator SoC Chips
- DVB-T
- ISDB-T
- DMTB
1. T2M
2. Wireless Products
3. Consumer Products
4. Interface Products
5. Contact Us
MIPI Interface controllers and PHY IP availability
# MIPI interface IP solutions

## 1. PHYS
- a. D-PHY-CSI2-TX
- b. D-PHY-CSI2-RX
- c. D-PHY-DSI-RX
- d. D-PHY-DSI-TX
- e. D-PHY
- f. M-PHY
- g. M-PHY-DigRF
- h. PHY-MMU-RX3
- i. PHY-MDDI

## 2. SERDES
- a. SRDS-4254
- b. SRDS-3204
- c. SRDS-2500
- d. SRDS-EPON
- e. SR-LVDS
- f. DS-LVDS
- g. SRDS-SGMII

## 3. PLL & DLL
- a. PLL-SYN
- b. PLL-SYN-LIF-DC
- c. PLL-MIPI
- d. PLL-MIPI-PXL
- e. PLL-CDR
- f. PLL-SS
- g. DLL

## 4. TRANSCEIVERS
- a. TXRX-MIPI
- b. TXRX-DigRF
- c. TXRX-MDDI
- d. TXRX-LVDS
- e. TXRX-DDR2
- f. TXRX-SSTL18
- g. TXRX-HSTL
- h. TXRX-CEATA
- i. TXRX-UCB
- j. TXRX-PATA
- k. TXRX-PCIX

## 5. ADC & DAC
- a. ADC9
- b. ADC10
- 6. ANALOG BLOCKS
  - a. BGR
  - b. BGRLV
  - c. AMUX
  - d. LVDET

## 6. ANALOG BLOCKS
- a. BGR
- b. BGRLV
- c. AMUX
- d. LVDET
USB, Memory, Multimedia and 8051

8051 Platform
The product line we have perfected for almost 15 years now. Since the development of the C8051 in 1997, we have already introduced 5 generations of 8051-compatible MCUs, each faster and more configurable than the other. The highlights of this line are:
- **R80251XC** - 32-bit 8051
- **R8051XC2** - Configurable 8051
- **T8051** - Tiny 8051

USB Controllers
For more than 10 years of USB IP development, we have developed controllers for all USB standards - SuperSpeed, High-Speed, Full-Speed and Low Speed. Our USB controller IP cores are silicon-proven, and vast majority is certified for USB compliance. Have a look at:
- **USBSS.DEV** - USB 3.0 Device controller
- **USBHS.PHY** - USB 2.0 PHY controller
- **USBHS.HUB** - USB 2.0 Hub controller

Memory Controllers
Our third, and most rapidly developing product line. Regularly updated for compliance with the latest specifications, our memory controllers feature dedicated software support and, in case of **NAND Flash**, a proprietary **SDLL PHY**. Please see the following:
- **NANDFLASH-CTRL** - NAND Flash IP
- **SDIO.HOST** - SD/SDIO/MMC Host
- **ATAIF** - Parallel ATA Controller

Multimedia
The most recent product line that embraces the latest Evatronix developments, like the JPEG-2000-4K Encoder or the budget 2K version with the reliable and proven IP for video and audio control. The featured products are:
- **JPEG 2000-4K** - Hi-end image encoder
- **DISPLAY.CTRL-4K** - DCI 4K compatible
- **I2S.SC** - single channel I2S controller
SDIO, USB, SLIMBUS

- **SDXC 3.0 – Host / Device Controller**
  - SDIO 3.0 Host IP provides supports for various system interfaces – VCI, AHB and OCP.
  - Number of slots[1/2] available is also configurable.
  - Provides UHS-I modes of operation - DS, HS, SDR12, SDR25, SDR50, SDR104 and DDR50.

- **SDIO2.0 – Host / Device Controller**
- **MIPI SLIMBUS – Host & Device**
- **USB3.0 Device**
  - Comes with USB3.0 to Gigabit reference design, class specific implementation does not need drivers
- **USB2.0 – Device / Host & OTG**
- **HDCP 2.0 – Used for content encryption over HDMI, USB**
- **10/100 Ethernet MAC – With TOE**
HDMI IP & Chip Portfolio

HDMI - IP

• Synthesizable Link Controller in Verilog RTL or Netlist Style
• Synthesis & STA Scripts
• Comprehensive Simulation Set with Testbench, Behavior Models, Scripts and Verification Data
• PHY Physical Design Database
• Detailed Technical Databook, Integration Manual, PCB Guideline and Other User Documents
• Reference Software Implementation

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Tx-1.3/1.4</th>
<th>Tx-1.4 LowPinCount</th>
<th>Tx-1.4 Single Power Supply</th>
<th>Rx-1.3/1.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>130G/110G</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>110-Hybrid</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>90G/85G</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>65G/55G(LP)</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>45G/40G(LP)</td>
<td>✔ / ✔</td>
<td>✔</td>
<td>(40LP)</td>
<td>13’Q2</td>
</tr>
<tr>
<td></td>
<td>28HPM</td>
<td>12’Q4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMIC</td>
<td>65LL/55LL</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>40LL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>12’Q3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GF/IBM</td>
<td>65G/55G</td>
<td>✔ / ✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>65LPe/55LPe</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UMC</td>
<td>130HS</td>
<td></td>
<td></td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>110-AI</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>65SP/55SP</td>
<td>✔ / ✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>65LL/55LL</td>
<td>✔ / ✔</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

✔: Silicon Proven  ✔: Pre-Silicon

HDMI TX LSI

• HDMI-1.3 24bit HDMI Transmitter
• HDMI-1.3 36bit HDMI Transmitter
UHS-II IP Portfolio

UHS-II: Serial Interface hard IP core using SerDes technology.

- Analog digital mixed design
- 1.5Gbs high speed design
- Serializer / Deserializer
- Low jitter clock synthesizer PLL
- Clock recovery PLL

SLI UHS-II PHY Features

- Hard analog part including I/O with soft digital part
- Support both Host and Device
- Low power and small area
  - 40mW@150MB/s, Full Duplex
- Up to 1.56Gbps/lane
- 300MB/s=3Gbps@Half Duplex
- 150MB/s@Full Duplex
- Clock synthesizer PLL, Data recovery, SerDes, BIST
- 8B10B coder / encoder
- 8b/16b selectable parallel I/F for Link

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Process</th>
<th>Host PHY</th>
<th>Device PHY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>130G/110G</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>110-Hybrid</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td>90G/85G</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td>65G/55G(LP)</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td>45G/40G(LP)</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>28HPM</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>SMIC</td>
<td>130/110G</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td>65/55LL</td>
<td></td>
<td>12’Q3</td>
</tr>
<tr>
<td></td>
<td>40LL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GF/IBM</td>
<td>65LPo/55LPo</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UMC</td>
<td>130HS</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>65LL/55LL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

✓: Silicon Proven  ✓: Pre-Silicon
NFC Radio Controller IP, Chip, Die

Unique features
- Lowest power consumption:
  - Power amplifier runs switch mode with an efficiency of 90%
  - The output power is dependent on the load, $P_{out}$ is variable
- Adaptive input attenuation.
  - Even with weak input signals no attenuation due to the switch-mode architecture and delivers good heat dissipation.
- Ultra low power wake-up detection.
- Anti-collision:
  - Passive mode - virtual anti-collision feature can select between different Secure Elements inside a mobile phone at the same time
  - Active mode - Can make selection and anti-collision between multiple cards

IP Offering
- Complete NFC Radio Controller IP
  - RF, Analog, Digital SW, Firmware
  - Die area 2mm$^2$ in 90nm CMOS (PADs not included)

Chip or Die Offering:
- 9 mm$^2$ (3.4mm x 2.7mm), QFN48
- Easy to mount NFC module containing all external components
  - 5.8mm x 7.7mm
- Evaluation kit
NFC Protocol Stack SW

- Full set of NFC Forum operations
- Fit in single or multithreaded environment
- Provides separate arbitration engine (Multiplexer)
- Supports different NFC interfaces and chips
- OS independent due to OSIF
- Runs on hardware without OS (e.g. modules)
- Follows Stollmann coding rules, protocol stack developing for more than 20 years
Security & Encryption IP Cores

**Ultra-Compact Cores**
- AES
- DES and 3DES
- AES Key Wrap
- Pseudo Random Generator
- True Random Generator
- SNOW 3G / Kasumi A5/3
- SHA
- Generic AES-CCM Core
- Combo GCM/CCM/EAX
- ZUC/EEA3/EIA3 Core

**High Throughput Cores**
- GCM (IEEE802.1ae)
- XTS (IEEE P1619)
- Combo XTS/GCM
- Combo XTS/GCM/CBC
- 10 Gbps Compression

**Communications Cores**
- WiMAX 802.16e CCM
- WiFi 802.11i CCM
- Zigbee CCM
- IEEE 802.15.3 CCM
- UWB MBOA CCM
- AES-CMAC/XCBC Core
- G.hn AES-CCM Core
- AES-CCM/CMAC Core
- WiFi CCMP/TKIP/RC4
- WAPI/SMS4 Processor

**Public Key Cores**
- RSA
- Elliptic (ECC)

**Compression**
- 10Gbps Compression
- Compression + Encryption
- Low Latency Compression

**Error Correction**
- Ethernet FEC Codec
- LDPC Codec

**Protocol Engines**
- IPsec Processor
- MACsec Processor
- IPsec/SSL/TLS Processor
- HDCP 2.0 Suite
- SSL/TLS with AXI Interface

**DSP Cores**
- 512/1024 Point FFT
- 64 Point FFT
- 32...4096 Point FFT
- Viterbi Detector
- FFT 32-512

**Legacy Cores**
- RC4
- LRW
- Combo GCM/LRW
Storage IP: Programmable SSD Flash Controller IP

- Customizable SSD Controller RTL IP
  - SATA 3.0 Interface Controller
  - AES Engine
  - Intelligent DMA controller and DDR3 Controller
  - 32 Bit Microprocessor
    - Managing up to 4 Flash Slice controllers
  - Each flash slice controller has
    - 4 Nandflash controllers, a CPU to manage the flash controllers
    - Flash controller has its own BCH syndrom generator
    - Each flash controllers supports up to 8 Chip select
    - Customizable BCH Syndrom polynomial and error correction logic
- Customizable with other Interfaces (PCIe 3.0)
- Portable to FPGA platforms
RISC Processor Cores

**Pollex3M-S**
- Synthesizable 32 bit low power RISC core single clock
  - 300 Mhz very small core (0.12 MM2 in 90nm)

**Pollex9**
- A synthesizable 32 bit low power Core single clock design
  - 400 Mhz 0.28MM2 in 90nm
  - 0.04 MW/Mhz

**Pollex7**
- A synthesizable 32 bit low power Core single clock design
  - 400 Mhz 0.21MM2 in 90nm
  - 0.05MW/Mhz

**RD80251**
- A high performance, opcode compatible core version of the industry standard 80251 micro controller

**RD8051**
- A high performance, opcode compatible core version of the industry standard 8051 micro controller

**AfricanBlue**
- A 32 Bit Java byte code compatible microprocessor core

**Table 1:**

<table>
<thead>
<tr>
<th>Process</th>
<th>MHz</th>
<th>Area (mm²)</th>
<th>Gate count</th>
<th>Power (mW/MHz)</th>
<th>Area (mm²)</th>
<th>Gate count</th>
<th>Power (mW/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.18µm</td>
<td>100</td>
<td>~0.63</td>
<td>~37.650</td>
<td>0.21</td>
<td>~0.87</td>
<td>~52.500</td>
<td>0.22</td>
</tr>
<tr>
<td>0.18µm</td>
<td>150</td>
<td>~0.69</td>
<td></td>
<td>0.21</td>
<td>~0.96</td>
<td></td>
<td>0.22</td>
</tr>
<tr>
<td>0.18µm</td>
<td>200</td>
<td>~0.83</td>
<td></td>
<td>0.23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.13µm</td>
<td>100</td>
<td>~0.30</td>
<td>~38.300</td>
<td>0.08</td>
<td>~0.43</td>
<td>~55.200</td>
<td>0.08</td>
</tr>
<tr>
<td>0.13µm</td>
<td>150</td>
<td>~0.36</td>
<td></td>
<td>0.09</td>
<td>~0.52</td>
<td></td>
<td>0.09</td>
</tr>
<tr>
<td>0.13µm</td>
<td>200</td>
<td>~0.42</td>
<td></td>
<td>0.11</td>
<td>~0.66</td>
<td></td>
<td>0.12</td>
</tr>
<tr>
<td>0.09µm</td>
<td>100</td>
<td>~0.15</td>
<td>~37800</td>
<td>0.03</td>
<td>~0.21</td>
<td>~52.100</td>
<td>0.03</td>
</tr>
<tr>
<td>0.09µm</td>
<td>200</td>
<td>~0.16</td>
<td></td>
<td>0.03</td>
<td>~0.23</td>
<td></td>
<td>0.03</td>
</tr>
<tr>
<td>0.09µm</td>
<td>300</td>
<td>~0.17</td>
<td></td>
<td>0.03</td>
<td>~0.24</td>
<td></td>
<td>0.03</td>
</tr>
<tr>
<td>0.09µm</td>
<td>400</td>
<td>~0.21</td>
<td></td>
<td>0.05</td>
<td>~0.28</td>
<td></td>
<td>0.04</td>
</tr>
</tbody>
</table>

Libraries used:
- SMIC 0.18µm Logic18 Process 1.8-Volt SAGE-XTM
- SMIC 130nm Logic013G Process 1.2-Volt SAGE-XTM v2.0
- SMIC 90nm LOGIC 90G RVT Process SAGE-XTM v3.0
DSP Processor Cores

WSP1600 DSP Core

• Full Compatibility to Popular ADSP-218X Architecture. It is a high-speed scalar (one instruction per clock cycle) 16-bit integer Digital Signal Processor optimized for audio, multimedia, consumer electronics, communications, and other high-speed signal processing applications.

• 3 Computational Units – ALU, MULT/MAC, & Shifter,
• 1 Program Sequencer, 2 Data Address Generators,
• 2 DMA Ports, 2 Serial Ports, 1 Programmable Timer,
• Flag I/Os, General Purpose I/Os,

WSP2416 DSP Core

• Full Compatibility to Popular ADSP-218X Architecture. It is a high-speed scalar (one instruction per clock cycle) 24/16-bit integer Dual-mode (24-bit & 16-bit mode) Digital Signal Processor optimized for audio, multimedia, consumer electronics, communications, and other high-speed signal processing applications.

• 3 Computational Units – ALU, MULT/MAC, & Shifter,
• 1 Program Sequencer, 2 Data Address Generators,
• 2 DMA Ports, 2 Serial Ports, 1 Programmable Timer,
• Flag I/Os, General Purpose I/Os,
1. T2M
2. Wireless Products
3. Consumer Products
4. Interface Products
5. Contact Us
Contact us for product information

David Salisbury
EMEA-Sales@t-2-m.com
+49-174-730-8410

Suresh S. Krishnan
ASIAN-Sales@t-2-m.com
+65-966-37470

Mark Ma
China-Sales@t-2-m.com
+86-135-246-280-96

Anil Mankar
US-Sales@t-2-m.com
+1-714-315-0995

Richard Wang
China-Sales@t-2-m.com
+86-138-1710-5679

HJ Kwon
Korea-Sales@t-2-m.com
+ 82-11-718-1046

Neil Mitchel
US-Sales@t-2-m.com
+1-408-656-9500

Colin Mason
Japan-Sales@t-2-m.com
+81-90-875-8419

Head Quarters
Info@t-2-m.com
+49-89-89-99-94-92

Angus Yen
Taiwan-Sales@t-2-m.com
+886-937-922972
Your Complex Technology Supplier

info@T-2-M.com